REMARKS

Applicant appreciates the Examiner's thorough review of the present application and the withdrawal of the previous rejections. The Office Action has, however, rejected claims 12-20 based on newly-cited art, and respectfully requests reconsideration of the rejections for at least the following reasons.

Claims 12-20 remain pending in the application. Claims 13-20 ultimately depend from independent claim 12, and therefore are considered to be in condition for allowance, for at least the same reasons as claim 12.

Claim 12 was rejected, according to the Office Action, under 35 U.S.C. 103(a) as allegedly unpatentable over AAPA (fig. 1a) in view of Huang (U.S. Pat. 6,507,121). However, Huang should not be considered as prior art for at least the following reasons: The cited U.S. Pat. 6,507,121 was issued Jan 14, 2003, and the parent application (Serial No. 09/952,651) of the present application was filed Sep 13, 2001, and the present application was filed Aug 27, 2003. The issue date of the cited U.S. Pat. 6,507,121 was within one year prior to the application date of the present application, not to mention that the issue date of the cited U.S. Pat. 6,507,121 was after the filing date of the parent application of the present application. According to 35 USC 103(c), the cited U.S. Pat. 6,507,121 should not be considered as prior art, as it is owned by the same assignee (Siliconware Precision Industries Co., Ltd.) as the present application. For at least this reason, the rejection should be withdrawn.

In addition, the claimed invention of the present application differs from the cited U.S. Pat. 6,507,121 in at least the aspects described below.

The cited U.S. Pat. 6,507,121 is intended to be an advance of certain prior systems (*see e.g.,* col 2, lines 28-45). During the reflowing process, in connecting a chip carrier 206 to a

substrate 202 via an array of solder balls 208, the chip carrier 206 is supported by at least three solder balls 208a having HMT (high-melting-temperature) cores 220 and being located on the periphery of the array of solder balls 208. This structure controls the collapse level of the array of solder balls 208, and the short-circuit between adjacent solder balls 208 is prevented.

The claimed embodiment of the present application is intended for a product in which a chip 2 (see Fig. 6) is connected to a chip carrier 7 having neither connection pads nor an insulation layer thereon. The claimed embodiment of the present application provides a product featuring direct connection of a chip to a chip carrier, such as a lead frame which has neither connection pads nor insulation layer thereon, while immunizing against the problems arising from the lack of a mechanism on the lead frame to limit solder flowing.

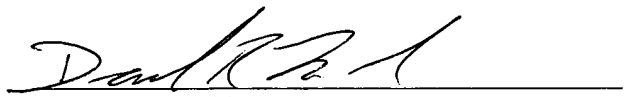
The features included in independent claim 12 are neither anticipated nor suggested by any prior art of which Applicant is currently aware. Accordingly, claim 12 patently defines over the cited art of record, and is in condition for allowance. Claims 13- 20 depend on claim 12, and all such dependent claims therefore are in condition for allowance and such action is respectfully requested.

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

By: 

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